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EXAMINER	
ORTIZ, EDGARDO	

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2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,701	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/353,282.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/2/04 & 5/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-12 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, 4, 5, 7, 8, 10, 11, 13, 14, 16 and 17 of U.S. Patent No. 6,822, 293 in view of U.S. Patent No. 5,845,166. For example and with regard to claim 1, U.S. Patent No. 6,822, 293 discloses:

a gate electrode formed over a substrate,

a first insulating layer formed over the gate electrode,

a second insulating layer formed over the first insulating layer,

a semiconductor layer formed over the second insulating layer, the

semiconductor layer having at least a channel region and at least one impurity

region,

an inorganic insulating layer formed over the semiconductor layer, the

inorganic insulating layer being in contact with a portion of the impurity region',

and

an organic insulating layer formed over the inorganic insulating layer,

the organic insulating layer being in contact with another portion of the

impurity region.

U.S. Patent No. 6,822, 293 fails to disclose the claimed camera elements of a main body; an eyepiece, a switching unit, an image receiver, and a display having a semiconductor device. However, U.S. Patent No. 5,845,166 discloses (figures 1-6) a camera including a main body (10), an eyepiece (20), a switching unit (39), an image receiver (126) and a display (36). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to include the claimed camera elements in combination with a semiconductor structure as disclosed by U.S. Patent No. 6,822, 293, in order to provide a camera device capable of using both a digital imaging system and a photographic imaging system (column 1, lines 6-8).

Claims 13-21 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-9 of U.S. Patent No. 6,822,293. Although the conflicting claims are not identical, they are not patentably distinct from each other because for example and with regard to claim 1, U.S. Patent No. 6,822,293 discloses:

a gate electrode formed over a substrate,

a first insulating layer formed over the gate electrode,

a second insulating layer formed over the first insulating layer,

a semiconductor layer formed over the second insulating layer, the semiconductor layer having at least a channel region and at least one impurity region,

an inorganic insulating layer formed over the semiconductor layer, the inorganic insulating layer being in contact with a portion of the impurity region, and

an organic insulating layer formed over the inorganic insulating layer, the organic insulating layer being in contact with another portion of the impurity region.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han (U.S. Patent No. 5,926,235) in view of Hwang (U.S. Patent No. 5,852,481) and further in view of Fellegara et al. (U.S. Patent No. 5,845,166). With regard to Claim 1, Han discloses (figure 5I) a gate electrode (107) formed over a substrate (110), an insulating layer (109) formed over the substrate, a semiconductor layer (111) formed over the insulating layer, the semiconductor layer having at least a channel (region between source/drain electrodes 105, 106) and at least one impurity region (see the region below portion 112), an inorganic insulating layer (113a) formed

over the semiconductor layer, the inorganic layer being in contact with a portion of the impurity region and an organic insulating layer (113b) formed over the inorganic insulating layer, the organic insulating layer being in contact with another portion of the impurity region.

Han fails to disclose the claimed first and second insulating layers formed over the gate electrode. Hwang discloses (figure 2B) first and second insulating layers (115, 116) comprising silicon oxide and silicon nitride, formed over a gate electrode (111). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Han to include the claimed first and second insulating layers formed over the gate electrode, as disclosed by Hwang, in order to provide first and second insulating layers to improve insulating and boundary characteristics (column 4, lines 43-46).

Regarding the claimed camera elements of a main body; an eyepiece, a switching unit, an image receiver, and a display having a semiconductor device, Fellegara discloses (figures 1-6) a camera including a main body (10), an eyepiece (20), a switching unit (39), an image receiver (126) and a display (36). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to include the claimed camera elements in combination with a semiconductor structure as disclosed by Han and Hwang, in order to provide a camera device capable of using both a digital imaging system and a photographic imaging system (column 1, lines 6-8).

With regard to Claim 2, Han discloses a gate electrode (107) comprising chromium (column 3, lines 63-67 and column 4, lines 1-4).

With regard to Claim 3, Han discloses (figure 5I) a gate electrode (107) formed over a substrate (110), an insulating layer (109) formed over the substrate, a semiconductor layer (111) formed over the insulating layer, the semiconductor layer having at least a channel (region between source/drain electrodes 105, 106) and at least one impurity region (see the region below portion 112), an inorganic insulating layer (113a) formed over the semiconductor layer, the inorganic layer being in contact with a portion of the impurity region and an organic insulating layer (113b) formed over the inorganic insulating layer, the organic insulating layer being in contact with another portion of the impurity region.

Han fails to disclose the claimed first and second insulating layers formed over the gate electrode. Hwang discloses (figure 2B) first and second insulating layers (115, 116) comprising silicon oxide and silicon nitride, formed over a gate electrode (111). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Han to include the claimed first and second insulating layers formed over the gate electrode, as disclosed by Hwang, in order to provide first and second insulating layers to improve insulating and boundary characteristics (column 4, lines 43-46).

Regarding the claimed camera elements of a main body; an eyepiece, a switching unit, an image receiver, and a display having a semiconductor device, Fellegara discloses (figures 1-6) a camera

including a main body (10), an eyepiece (20), a switching unit (39), an image receiver (126) and a display (36). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to include the claimed camera elements in combination with a semiconductor structure as disclosed by Han and Hwang, in order to provide a camera device capable of using both a digital imaging system and a photographic imaging system (column 1, lines 6-8).

With regard to Claim 4, Han discloses a gate electrode (107) comprising chromium (column 3, lines 63-67 and column 4, lines 1-4).

With regard to Claim 5, Han discloses (figure 5I) a gate electrode (107) formed over a substrate (110), an insulating layer (109) formed over the substrate, a semiconductor layer (111) formed over the insulating layer, the semiconductor layer having at least a channel (region between source/drain electrodes 105, 106) and at least one impurity region (see the region below portion 112), an inorganic insulating layer (113a) formed over the semiconductor layer, the inorganic layer being in contact with a portion of the impurity region and an organic insulating layer (113b) formed over the inorganic insulating layer, the organic insulating layer being in contact with another portion of the impurity region.

Han fails to disclose the claimed first and second insulating layers formed over the gate electrode. Hwang discloses (figure 2B) first and second insulating layers (115, 116) comprising silicon oxide and silicon nitride, formed over a gate electrode (111). Therefore, it would have

been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Han to include the claimed first and second insulating layers formed over the gate electrode, as disclosed by Hwang, in order to provide first and second insulating layers to improve insulating and boundary characteristics (column 4, lines 43-46).

Regarding the claimed camera elements of a main body; an eyepiece, a switching unit, an image receiver, and a display having a semiconductor device, Fellegara discloses (figures 1-6) a camera including a main body (10), an eyepiece (20), a switching unit (39), an image receiver (126) and a display (36). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to include the claimed camera elements in combination with a semiconductor structure as disclosed by Han and Hwang, in order to provide a camera device capable of using both a digital imaging system and a photographic imaging system (column 1, lines 6-8). Additionally, the claimed thickness for the first and second insulating layers would have been obvious to one of ordinary skill in the art at the time the invention was made to, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. In the instant case, such a modification optimizes the overall size of the semiconductor device.

With regard to Claim 6, Han discloses a gate electrode (107) comprising chromium (column 3, lines 63-67 and column 4, lines 1-4).

With regard to Claim 7, Han discloses (figure 5I) a gate electrode (107) formed over a substrate (110), an insulating layer (109) formed over the substrate, a semiconductor layer (111) formed over the insulating layer, the semiconductor layer having at least a channel (region between source/drain electrodes 105, 106) and at least one impurity region (see the region below portion 112), an inorganic insulating layer (113a) formed over the semiconductor layer, the inorganic layer being in contact with a portion of the impurity region and an organic insulating layer (113b) formed over the inorganic insulating layer, the organic insulating layer being in contact with another portion of the impurity region.

Han fails to disclose the claimed first and second insulating layers formed over the gate electrode. Hwang discloses (figure 2B) first and second insulating layers (115, 116) comprising silicon oxide and silicon nitride, formed over a gate electrode (111). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Han to include the claimed first and second insulating layers formed over the gate electrode, as disclosed by Hwang, in order to provide first and second insulating layers to improve insulating and boundary characteristics (column 4, lines 43-46).

Regarding the claimed camera elements of a main body; an eyepiece, a switching unit, an image receiver, and a display having a semiconductor device, Fellegara discloses (figures 1-6) a camera including a main body (10), an eyepiece (20), a switching unit (39), an image receiver (126) and a display (36). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to include the claimed camera elements in combination with a

semiconductor structure as disclosed by Han and Hwang, in order to provide a camera device capable of using both a digital imaging system and a photographic imaging system (column 1, lines 6-8).

With regard to Claim 8, Han discloses a gate electrode (107) comprising chromium (column 3, lines 63-67 and column 4, lines 1-4).

With regard to Claim 9, Han discloses (figure 5I) gate electrodes (107), it is noted that Han discloses an active matrix liquid crystal display comprising thin film transistors (column 1, lines 5-9) and thus there is a plurality of gate electrodes formed over a substrate (110), an insulating layer (109) formed over the substrate, a semiconductor layer (111) formed over the insulating layer, the semiconductor layer having at least a channel (region between source/drain electrodes 105, 106) and at least one impurity region (see the region below portion 112), an inorganic insulating layer (113a) formed over the semiconductor layer, the inorganic layer being in contact with a portion of the impurity region and an organic insulating layer (113b) formed over the inorganic insulating layer, the organic insulating layer being in contact with another portion of the impurity region.

Han fails to disclose the claimed first and second insulating layers formed over the gate electrode. Hwang discloses (figure 2B) first and second insulating layers (115, 116) comprising silicon oxide and silicon nitride, formed over a gate electrode (111). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the

structure as disclosed by Han to include the claimed first and second insulating layers formed over the gate electrode, as disclosed by Hwang, in order to provide first and second insulating layers to improve insulating and boundary characteristics (column 4, lines 43-46).

Regarding the claimed camera elements of a main body; an eyepiece, a switching unit, an image receiver, and a display having a semiconductor device, Fellegara discloses (figures 1-6) a camera including a main body (10), an eyepiece (20), a switching unit (39), an image receiver (126) and a display (36). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to include the claimed camera elements in combination with a semiconductor structure as disclosed by Han and Hwang, in order to provide a camera device capable of using both a digital imaging system and a photographic imaging system (column 1, lines 6-8).

With regard to Claim 10, Han discloses a gate electrode (107) comprising chromium (column 3, lines 63-67 and column 4, lines 1-4).

With regard to Claim 11, Han discloses (figure 5I) gate electrodes (107), it is noted that Han discloses an active matrix liquid crystal display comprising a plurality of thin film transistors (column 1, lines 5-9), a gate electrode formed over a substrate (110), an insulating layer (109) formed over the substrate, a semiconductor layer (111) formed over the insulating layer, the semiconductor layer having at least a channel (region between source/drain electrodes 105, 106) and at least one impurity region (see the region below portion 112), an inorganic insulating layer

(113a) formed over the semiconductor layer, the inorganic layer being in contact with a portion of the impurity region and an organic insulating layer (113b) formed over the inorganic insulating layer, the organic insulating layer being in contact with another portion of the impurity region.

Han fails to disclose the claimed first and second insulating layers formed over the gate electrode. Hwang discloses (figure 2B) first and second insulating layers (115, 116) comprising silicon oxide and silicon nitride, formed over a gate electrode (111). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Han to include the claimed first and second insulating layers formed over the gate electrode, as disclosed by Hwang, in order to provide first and second insulating layers to improve insulating and boundary characteristics (column 4, lines 43-46).

Regarding the claimed camera elements of a main body; an eyepiece, a switching unit, an image receiver, and a display having a semiconductor device, Fellegara discloses (figures 1-6) a camera including a main body (10), an eyepiece (20), a switching unit (39), an image receiver (126) and a display (36). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to include the claimed camera elements in combination with a semiconductor structure as disclosed by Han and Hwang, in order to provide a camera device capable of using both a digital imaging system and a photographic imaging system (column 1, lines 6-8).

With regard to Claim 12, Han discloses a gate electrode (107) comprising chromium (column 3, lines 63-67 and column 4, lines 1-4).

Claims 13-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han (U.S. Patent No. 5,926,235) in view of Hwang (U.S. Patent No. 5,852,481). With regard to Claim 13, With regard to Claim 1, Han discloses (figure 5I) a gate electrode (107) formed over a substrate (110), an insulating layer (109) formed over the substrate, a semiconductor layer (111) formed over the insulating layer, the semiconductor layer having at least a channel (region between source/drain electrodes 105, 106) and at least one impurity region (see the region below portion 112), an inorganic insulating layer (113a) formed over the semiconductor layer, the inorganic layer being in contact with a portion of the impurity region and an organic insulating layer (113b) formed over the inorganic insulating layer, the organic insulating layer being in contact with another portion of the impurity region.

Han fails to disclose the claimed first and second insulating layers formed over the gate electrode. Hwang discloses (figure 2B) first and second insulating layers (115, 116) comprising silicon oxide and silicon nitride, formed over a gate electrode (111). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Han to include the claimed first and second insulating layers formed over the gate electrode, as disclosed by Hwang, in order to provide first and second insulating layers to improve insulating and boundary characteristics (column 4, lines 43-46).

With regard to Claim 14, Han discloses a gate electrode (107) comprising chromium (column 3, lines 63-67 and column 4, lines 1-4).

With regard to Claim 16, Han discloses (figure 5I) a gate electrode (107) formed over a substrate (110), an insulating layer (109) formed over the substrate, a semiconductor layer (111) formed over the insulating layer, the semiconductor layer having at least a channel (region between source/drain electrodes 105, 106) and at least one impurity region (see the region below portion 112), an inorganic insulating layer (113a) formed over the semiconductor layer, the inorganic layer being in contact with a portion of the impurity region and an organic insulating layer (113b) formed over the inorganic insulating layer, the organic insulating layer being in contact with another portion of the impurity region.

Han fails to disclose the claimed first and second insulating layers formed over the gate electrode. Hwang discloses (figure 2B) first and second insulating layers (115, 116) comprising silicon oxide and silicon nitride, formed over a gate electrode (111). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Han to include the claimed first and second insulating layers formed over the gate electrode, as disclosed by Hwang, in order to provide first and second insulating layers to improve insulating and boundary characteristics (column 4, lines 43-46).

With regard to Claim 17, Han discloses a gate electrode (107) comprising chromium (column 3, lines 63-67 and column 4, lines 1-4).

With regard to Claim 19, Han discloses (figure 5I) a gate electrode (107) formed over a substrate (110), an insulating layer (109) formed over the substrate, a semiconductor layer (111) formed over the insulating layer, the semiconductor layer having at least a channel (region between source/drain electrodes 105, 106) and at least one impurity region (see the region below portion 112), an inorganic insulating layer (113a) formed over the semiconductor layer, the inorganic layer being in contact with a portion of the impurity region and an organic insulating layer (113b) formed over the inorganic insulating layer, the organic insulating layer being in contact with another portion of the impurity region.

Han fails to disclose the claimed first and second insulating layers formed over the gate electrode. Hwang discloses (figure 2B) first and second insulating layers (115, 116) comprising silicon oxide and silicon nitride, formed over a gate electrode (111). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Han to include the claimed first and second insulating layers formed over the gate electrode, as disclosed by Hwang, in order to provide first and second insulating layers to improve insulating and boundary characteristics (column 4, lines 43-46). Additionally, the claimed thickness for the first and second insulating layers would have been obvious to one of ordinary skill in the art at the time the invention was made to, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. In the instant case, such a modification optimizes the overall size of the semiconductor device.

With regard to Claim 20, Han discloses a gate electrode (107) comprising chromium (column 3, lines 63-67 and column 4, lines 1-4).

Claims 15, 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han (U.S. Patent No. 5,926,235) in view of Hwang (U.S. Patent No. 5,852,481) and further in view of Fellegara et al. (U.S. Patent No. 5,845,166). With regard to Claim 15, 18 and 21, Han and Hwang essentially disclose the claimed invention but fail to disclose that the semiconductor device is selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle-type display, a player for a recording medium, a digital still camera, a front-type projector and a rear-type projector. However, Fellegara discloses (figures 1-6) a digital-camera including a main body (10) and a liquid crystal display status unit (22) provided on the top of the main camera body. The ordinary artisan would recognize that an LCD device comprises thin-film transistors as part of its structure. Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to select a digital-still-camera as the semiconductor device using the elements disclosed by Han and Hwang, in order to provide a camera device capable of using both a digital imaging system and a photographic imaging system (column 1, lines 6-8).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O
A.U. 2815
3/31/05

GEORGE ECKERT
PRIMARY EXAMINER